WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array having electrically rewritable nonvolatile memory cells arranged therein;

a plurality of latch circuits which temporarily hold data read out from said memory cell array;

a first circuit which is configured to generate a first current varying in proportion to "1" or "0" of binary logical data of one end of said plurality of latch circuits;

a second circuit which is configured to generate a second preset current; and

a third circuit which is configured to compare the first current with the second current;

wherein the number of "1" or "0" of binary logical data of one end of said plurality of latch circuits is detected based on the result of comparison between the first current and the second current.